Hadassah Academic College
Department of Computer Science

Advanced Computer Architecture Exercise 6

1. An OLTP server receives independent request and generates a separate thread for each request. The thread instructions are stored in a shared Reorder Buffer and execute by dynamic scheduling. The superscalar CPU can execute 4 instructions per clock cycle. The CPU attempts to advance each thread equally.

   OLTP requests require database access, causing cache misses, page faults, and so on. Assume that 8 threads are running, that each thread runs 4 instructions before a stall of 3 clock cycles (caused by memory latency) and then runs 4 more instructions. For each thread that is not stalled, 2 instructions can be found to run in parallel.

   Show the progress of the system according to thread number, continuing the example, up to clock cycle 12.

CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8	CC9	CC10	CC11	CC12
1	3	5									
1	3	5									
2	4	6									
2	4	6									

2. A one-loop program is running on an SMP computer with N CPUs. Each CPU receives an equal-sized chunk of the index range of size L in the loop, so that the number of interactions in any CPU is L/N.

   Communications overhead is follows from the clock cycles required to distribute the loop code separately to each CPU, so that

$$CC^{comm} = \text{communication overhead clock cycles} = CPIPP \times IC^{loop} \times N$$

$$CPIPP = \text{clock cycles per instruction per processor}$$

$$IC^{loop} = \text{number of instructions in loop}$$

   A. Write an expression for $CC^{execute}$ = cycles to distribute and execute the code in the CPUs.

   B. Find the speedup (relative to a single thread) as a function of N.

   C. Find $N^{optimum}$ = the number of threads that minimizes the run time.

   D. Find the speedup (relative to a single thread) for $N^{optimum}$.

   E. Find $CC^{execute}$ for $N^{optimum}$.

   F. Find the number of loop iterations per CPU L/N for $N^{optimum}$.