Hadassah Academic College
Department of Computer Science

Advanced Computer Architecture — Exercise 4

1. Consider the following code fragment:

```
 0        ADDI R1, R0, #0x60
 1  L1:   SUBI R1, #4
 2        LW R2, 0(R1)
 3        LW R3, 0x1000(R1)
 4        ADD R4, R2, R3
 5        SW 2000(R1), R4
 6        SGT R5, R2, R3          ; R5 ← 1 if R2 > R3, else R5 ← 0
 7        BNEZ R5, L2             ; if R5 != 0 jump L2 (jump if R2 > R3)
 8        BNEZ R1, L1             ; if R1 != 0 jump L1
          END
 9  L2:   LW R6, 0x400(R0)
10        ADDI R6, R6, #1
11        SW 0x400(R0), R6
12        BNEZ R1, L1             ; if R1 != 0 jump L1
```

The data in memory is

```
regs[R2] = regs[R1] % 0x40
regs[R3] = regs[R1] % 0x10
```

A. Build a table that shows the history of each branch instruction in the running of the code, according to the changing values of registers R1, R2, R3.

R1	R2	R3	R2 > R3	line 7	line 8	line 12
5C	1C	0C	1	1	—	1
58	18	08	1	1	—	1

Using the Yeh-Patt algorithm for line 7 and the execution in part A.

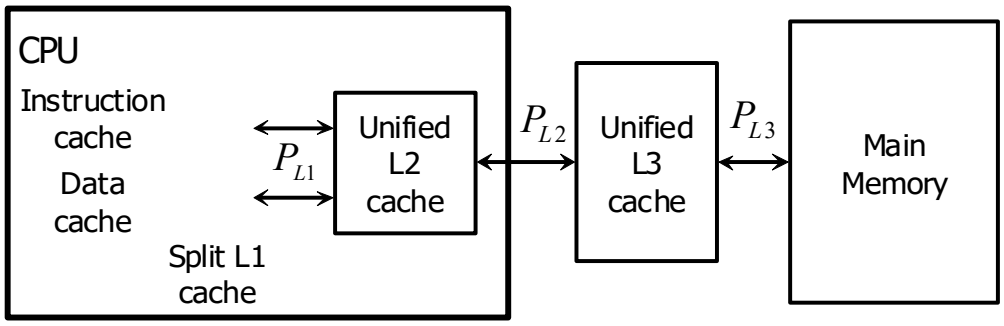
B. Write the 4-bit BHR.

C. Write the state of the 2-bit PHT at the end of the execution and the predictions of a 2-bit counter. Compare the predictions with the actual branch behavior.

D. Write the state of the 2-bit PHT at the end of the execution and the predictions of a 4-bit counter. Compare the predictions with the actual branch behavior.

2. A certain CPU has a 3-level cache as follows:

Level	Split/Unified	Miss Rate(s)	Miss Penalty
L1	Split	M^{I}_{L1} , M^{D}_{L1}	P_{L1}
L2	Unified	M_{L2}	P_{L2}
L3	Unified	M_{L3}	P_{L3}



A. Generalizing the expressions

$$CPI_{1-level}^{stall} = \left[M_{L1}^{I} + M_{L1}^{D} \times \frac{IC^{A}}{IC} \right] \times P_{L1}$$

$$CPI_{2-level}^{stall} = \left[M_{L1}^{I} + M_{L1}^{D} \times \frac{IC^{A}}{IC} \right] \times \left(P_{L1} + M_{L2} \times P_{L2} \right)$$

write (without a formal proof) a formula for $CPI_{3-level}^{stall}$ and explain why your expression is reasonable.

B. Using the expression for $CPI_{3-level}^{stall}$ and the values in the table

Level	Split/Unified	Miss Rate(s)	Miss Penalty
L1	Split	M^{I}_{L1} = 1 % M^{D}_{L1} = 5 %	P_{L1} = 5 cycles
L2	Unified	M_{L2} = 1 %	P_{L2} = 5 cycles
L3	Unified	M_{L3} = 1 %	P_{L3} = 50 cycles

$$\frac{IC^{A}}{IC} = 0.40$$

compare the results with the $CPI_{2-level}^{stall}$ using the values in this table (a 2 level cache a large miss penalty at L2).

Level	Split/Unified	Miss Rate(s)	Miss Penalty
L1	Split	M^{I}_{L1} = 1 % M^{D}_{L1} = 5 %	P_{L1} = 5 cycles
L2	Unified	M_{L2} = 1 %	P_{L2} = 50 cycles