Hadassah Academic College
Department of Computer Science

Advanced Computer Architecture Exercise 3

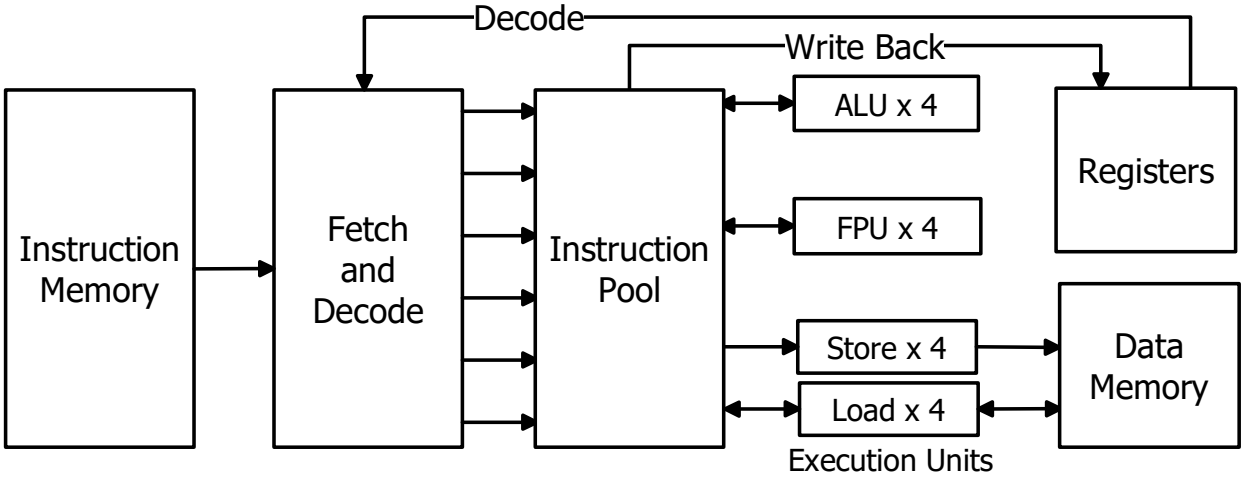
All questions related to the following code fragment:

```
     ADDI R1, R0, #400
     LF F0, #1000(R1)     ; load float to FP register F0
L1:  SUBI R1, R1, #8
     LF F1, 0(R1)
     ADDF F1, F1, F0      ; add float
     SF 0(R1), F1
     LF F1, 4(R1)
     SUBF F1, F1, F0      ; subtract float
     SF 4(R1), F1
     BNEZ R1, L1          ; branch to L1 if Regs[R1] ≠ 0
```

1. Show, as in slide 60 of Chapter 3, the stages of execution of the first loop iteration in a standard DLX. Assume that the FPU operates on floating point just as the ALU operates on integers (performs addition and subtraction in one clock cycle).

The CPU in the illustration performs dynamic scheduling as in the x86 model expanded to 4 instructions of each type (ALU ,FPU ,Load ,Store) on each clock cycle.

2. How many times does the instruction at label L2 run?



2. Show the stages of execution of the first loop iteration on this CPU, without register renaming. Find the speedup with respect to the result of question 1.
3. Repeat question 2 using register renaming. Find the speedup with respect to the result of question 1.
4. Repeat question 3 also using $\times$ 2 loop unrolling. Find the speedup with respect to the result of question 1.
5. Repeat question 4 also using software pipelining (assuming required changes to the CPU). Find the speedup with respect to the result of question 1.